AMENDMENTS TO THE DRAWINGS

Please enter the four (4) replacement sheets for drawings sheets 1/13, 7/13, 8/13 and 9/13, which include Amendments to Figs 1, 10, 11 and 12, respectively. The changes effected therein are shown by the red-line markings in the accompanying annotated sheets corresponding thereto. The replacement sheets are enclosed herewith as Appendix A and the annotated sheets are enclosed here with as Appendix B. The amendments to the drawings include the following:

In Fig. 1, the referred to read-out switch 61 in paragraphs [0045], [0050], etc., in the Substitute Specification, is now labeled therein; also in Fig. 1, the described data lines 22, referred to on page 8, paragraph [0032], is now labeled in Fig. 1 (this is also consistent with Fig. 7 of the drawings and the related description thereto).

In Fig. 10, diode 62 was re-labeled as 63. (This change was effected to avoid conflict with the numerical character 62 which represents the memory cell in Fig. 9.)

In Fig. 11, numerals 63 and 64 were replaced with numerals 64 and 65, respectively. (These changes were made in view of the change effected in Fig. 10.)

In Fig. 12, the numerical character 67 was added in connection with the latch circuit of the same number described on page 26, paragraph [0067], of the Substitute Specification.

Remarks

Withdrawal of the finality of the last Office Action and acceptance/formal entry of this Submission (Amendment) pursuant to USPTO RCE (Request for Continued Examination) practice is respectfully requested. Also, reconsideration and favorable action of the above-identified application, as currently amended, is respectfully requested.

Acceptance/formal entry of the above-listed four (4) replacement sheets of drawings, which contain remedial changes to Figs. 1, 10, 11 and 12, is respectfully requested. These changes are described above in the listings of the Amendments to the Drawings. It is submitted, these changes are strictly of a minor formal/remedial nature and include a change to remove the informality noted in Item 1 on page 2 of the final Office Action.

By the above-made amendments, also, claims 1 – 39 are now pending, of which claims 1, 8, 10, 19, 28, 29, 31 – 33 and 35 – 37 were amended and independent claim 39 is being newly presented. The amendments effected in the previously pending claims are strictly of a minor editorial nature. For example, in independent claim 1, the expression "each of said display pixels having a pixel electrode and pixel switch..." was amended to the expression "each of said of display pixels comprising a pixel electrode and a pixel switch...". Similar such changes were effected, also, in the other independent claims. It is submitted, this change is strictly of an editorially formatting nature. Also, the expression "said memory element" was appropriately amended to the expression "a memory element" with regard to independent claims 1, 29, 31 – 33 and 35 – 37. The revision effected in dependent claim 8 is strictly to remove a typographically informality. In claim 10, the revision therein is strictly to avoid conflict with the referred to "pixel switch" of intervening claim 6. The expression " said memory

capacitor" in dependent claim 10 is part of a memory element, for example, of the frame memory of the disclosed display apparatus, which is different from the display pixel portion thereof. In other words, the poly-Si TFT of claim 10 is different from that of the poly-Si TFT of claim 5, which pertains to a pixel in the pixel display. The revisions implemented in dependent claim 19 are of an obvious editorially clarifying nature, consistent with that shown in the drawings (e.g. Fig. 10, etc. and related discussion in the Substitute Specification).

Newly added independent claim 39 is based on subject matter covered in independent claim 1, etc., although somewhat modified therefrom. Specifically, this claim has been drafted to particularly highlight that the memory elements which store digital display data are multi-bit memory elements, examples of which are the three-bit memory elements shown in the numerous example embodiments disclosed in the present application, although not limited thereto. For example, in the first embodiment of a LCD panel shown in Fig. 1 of the drawings and described beginning on page 8, paragraph [0030], of the Substitute Specification, each of the memory cells 11 of the frame memory is a three unit memory element and is referred to in the Specification as three basic units of the memory element. Fig. 2 details a basic unit of a three-bit memory cell 11, which constitutes three bits of digital image data. (Page 10, paragraph [0034], of the Substitute Specification.) Therefore, the digital display data, which is stored in the memory elements such as in connection with the frame memory, involves the storing of three bits of digital data in respective ones of the memory elements thereof, according to new claim 39.

In the previously standing final Office Action, claims 1 – 27 and 29 – 38 were rejected under 35 U.S.C. 112, first paragraph, for the reasons that the claims "[fail] to comply with the written description requirement." Specifically, it is alleged in this rejection that the original disclosure in the Specification does not support the set

forth limitation "a plurality of memory elements for storing digital display data," with regard to independent claims 1, 29, 31 – 33 and 35 – 37. On the basis of this, these independent claims as well as their corresponding dependent claims thereof, stand finally rejected. However, as shown below, supportive disclosure is found in the original Specification and related drawings. Therefore, insofar as presently applicable, this rejection is traversed and reconsideration and withdrawal of the same is respectfully requested.

According to the example first embodiment of the original disclosure and the discussion of related Figs. 1+, each of the memory cells 11of the frame memory is shown to contain three basic units, each unit being specifically discussed with regard to Fig. 2 of the drawings, etc. For example, on page 10, paragraph [0034], of the Substitute Specification (or page 9, lines 16 – 18, of the original Specification), the inventors state that "memory cell is composed of three basic units, as shown in Fig. 2, but this is because the image data handled here is three bits." (emphasis added) It is noted that in the other example embodiments of an image display apparatus according to the present invention, multi-bit memory elements are, likewise, also employed in the frame memory. It is clearly apparent from the context of the discussion in the Specification of the operation of embodiment 1 (see Fig. 8) that the multi-bit memory elements thereof store digital display data (i.e., three-bit data stored in a memory cell). Therefore, reconsideration and withdrawal of the rejection under §112, first paragraph, for at least the above reasons, is respectively requested.

Claims 1, 9, 11, 14 – 17, 21 – 23, 25 and 29 – 38 stand rejected under 35 U.S.C. 103(a) over the combination of Yamaguchi, et al. (U.S. Patent 5,627,557) in view of Booth, Jr., et al. hereinafter "Booth, et al." (U.S. Patent 6,642,945); claims

2 – 8, 10, 18 – 20, 24 and 27 stand rejected over the combination of Yamaguchi, et al. and Booth, et al., as applied to claim 1 and further in view of Parks (U.S. Patent 5,471,225); and claim 28 stands rejected under 35 U.S.C. 103(a) over the combination of Yamaguchi, et al. in view of Zhang, et al. (U.S. Patent 6,611,261). As will be shown below, the invention set forth in claims 1 – 38 and, also, according to new claim 39 could not have been realized in the manner alleged in these rejections. Therefore, insofar as presently applicable, these rejections are traversed and reconsideration and withdrawal of the same is respectfully requested.

It is asserted in the rejection that Yamaguchi, et al. discloses all of the set forth featured aspects of claim 1 except, essentially, for "a refreshing operation means for performing a preset refreshing operation to [rewrite the] signal charge stored in the memory capacitor." Regarding "the refresh", Yamaguchi, et al. discloses a concept in which new data is written in the picture element (the pixel). Yamaguchi, et al.'s scheme, it is noted, is intended for "an analog memory" and that written-in data is data rewritten newly.

It is submitted, storage levels associated with an analog memory such as typified in Yamaguchi et al. leads to loss of data resulting from leakage current over time. On the other hand, in accordance with the present invention, each basic unit associated with the memory element comprises a memory switch, a memory capacity connected to the memory switch, an amplifier FET and refreshing operation means for performing a preset refreshing operation to rewrite a signal charge stored in the memory capacitor using the amplifier FET, the signal charged stored being in the form of digital display data. An example description regarding the performing of a preset refreshing operation to rewrite stored digital data in a multi-bit memory element as that shown in Figs. 1 and 2, although not limited thereto, is described in connection with reference to Fig. 8 of the drawings.

Booth is cited as teaching the following:

> "a display panel (100) including an array (106) of liquid crystal display pixel cells (125). Each of the pixel cells (125) may be part of a display element (120), a circuit that stores a change that indicates an intensity of a pixel that is formed by the pixel cell (see column 3, lines 32-49). An update circuit (130) includes a storage unit (124) that stores the terminal voltage across the associated pixel cell (125) after each update. That is the storage unit (123) includes a capacitor (142) that has a much larger capacitance than the capacitor of the pixel cell (125). The display panel may use the storage units (124) to regularly refresh the pixel cells (125) automatically without receiving new image data. Booth also teaches that each storage unit (124) may include a transistor that is activated to couple the capacitor (142) to the pixel cell (125) to refresh the terminal voltage across the pixel cell (125 (see column 5, lines 6-42)."

Based on the above, it is alleged in the final rejection that "it would have been obvious...to allow the usage of the update circuit including the capacitor for refreshing the voltages in the pixel cell arrangement which is taught by Booth, in a device...taught by Yamaguchi et al..." to realize the invention according to base claim 1.

Booth et al., discloses a scheme in which the loss of analog data, caused by leak current over time, is mitigated. However, according to Booth et al., the display panel (see Figs. 5 and 6) is such that a terminal voltage of a pixel uses analog memory and that written-in data is rewritten newly. In other words, Booth et al., Applicants submit, does not teach a refreshing operation scheme for performing a preset refreshing operation to rewrite stored digital display data in the manner as that set forth in base claim 1 and further according to the corresponding dependent thereof. The "refresh" operation intended by Booth, et al is not to recover the lost signal, but to mitigate the vanishing (the lost) of the analog signal voltage. As a result, Booth et al provides no mechanism to recover data or reliably rewrite data, and the analog signal voltage will be lost in time due to a leak current.

It is submitted, Booth et al. fails to teach a memory element construction in which the memory elements store digital display data and in which the memory elements are structured as that presently set forth in claims 1+. That is Booth et al's scheme does not lead to recovering data that is lost as a result of leakage current with lapse of time. In accordance with the present invention, however, the concept of a preset refreshing operation in the digital memory resides in the recovery by rewriting-in the data, which becomes lost as a result of leakage current from a lapse of time. The recovery is with regard to the writing in of data that is lost. This concept is set forth in each of independent claims 1, 29, 31-33 and 35-37, for example, in connection with the set forth "refreshing operation means for performing a preset refreshing operation to rewrite a signal charge stored in said memory capacitor." It is submitted, since the memory according to the present invention is a digital memory, it then becomes possible to perform lasting regeneration (i.e., a continuing regeneration of the storage state). This can be referred to as the rewriting operation for the rewriting function. Accordingly, it becomes possible to rewrite the data surely, i.e., data which becomes lost as a result of leakage current with lapse of time. For purposes of this response, the earlier supportive discussion/rebuttal arguments presented regarding the applicability of Yamaguchi et al. and Booth et al. to Applicants invention, which was submitted in the responsive remarks of the previous amendment, is also incorporated herein.

The invention according to dependent claims 2-8, 10, 18-20, 24 and 27 is also considered patentable, even when Yamaguchi et al and Booth et al are combined with Parks, for the same and similar reasons as that argued above. In this regard it is noted that Parks was cited concerning pixel construction and other structural particulars of a liquid crystal display. That is the above deficiencies

regarding the combined teachings of Yamaguchi et al. and Booth et al. are not overcome even in view of the further teachings of Parks.

Regarding the image display apparatus according to independent claim 28, a featured aspect thereof calls for the set forth "reference voltage generating circuit" of the "image signal generating means" to use a boron-doped poly-Si thin-film resistor. Such, however, is not taught even in view of the combined teachings of Yamaguchi et al. and Zang et al. In this regard, it is noted that Zang et al. uses polycrystal Si thin film. As correctly noted in the rejection, Yamaguchi fails to teach a display apparatus in which the image signal generating means has a reference voltage generating circuit using a boron-doped poly-Si thin-film resistor to achieve a gray scale voltage generating resistor. In fact, even if one of ordinary skill would have applied the teachings of Yamaguchi et al. and Parks in combination, there still would not have been realized a schemed image display apparatus as that set forth in independent claim 28. Applicants would also like to emphasize that using a poly-Si thin-film resistor doped with boron leads to unexpected favorable results as that compared with phosphorus-doped poly-Si material in the formation of the thin film resistor (see page 11, paragraph [0040] to page 14, and Table 2 of the Substitute Specification or, alternatively, from page 10, line 26, to page 12, line 22, and Table 2 of the original specification).

The above discussion regarding claim 1 is also applicable with regard to newly presented claim 39. For at least the above reasons, the invention could not have been rendered obvious in the manner as that alleged in the outstanding rejections.

Therefore, in view of the amendments presented above together with these accompanying remarks, withdrawal of the outstanding rejections as well as

favorable action on the currently pending claims and an earlier formal notification of allowance of the above-identified application is respectfully requested.

To the extent necessary, applicants petition for an extension of time under 37 CFR §1.136. Please charge any shortage in the fees due in connection with the filing of this paper, including Extension of Time fees, to the Deposit Account of Antonelli, Terry, Stout & Kraus, LLP, Dep. Acct. No. 01-2135 (503.40029X00), and please credit any excess fees to such deposit account.

Respectfully submitted,
ANTONELLI, TERRY, STOUT & KRAUS, LLP

Larry N. Anagnos
Reg. No. 32,392

LNA/gjb
703-312-6600

FIG. 1

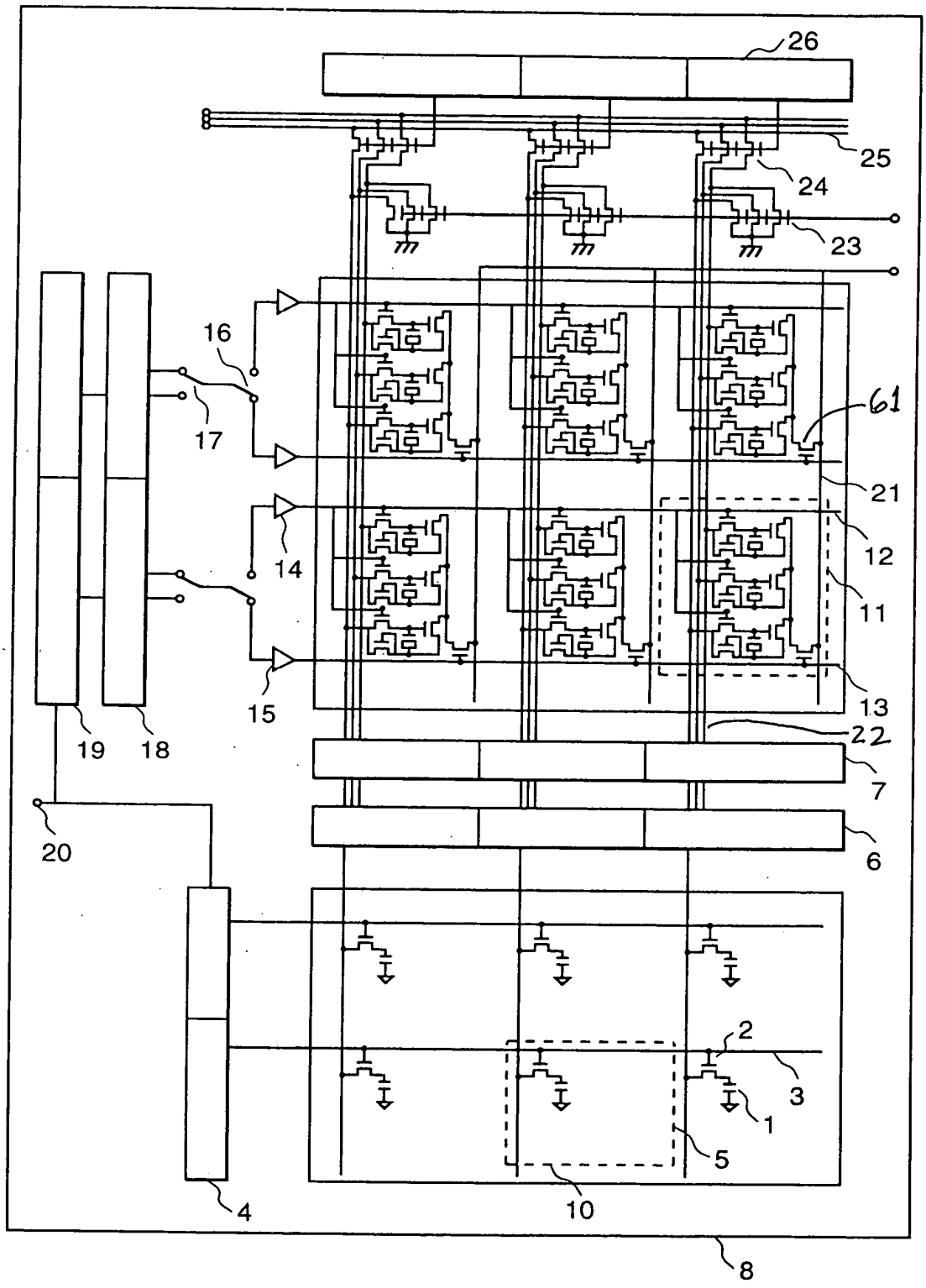

FIG. 10

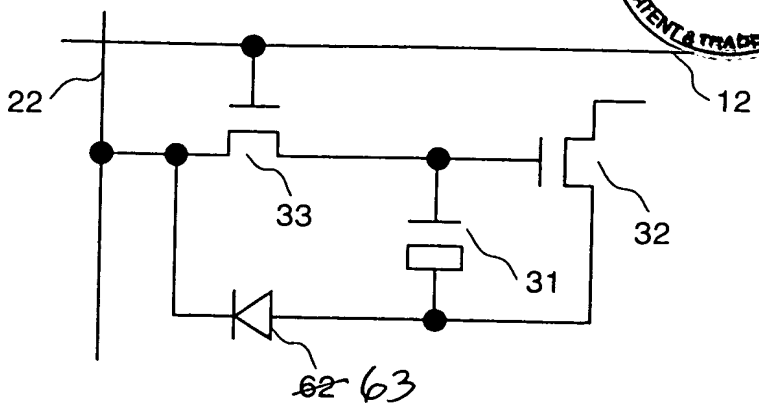

FIG. 13

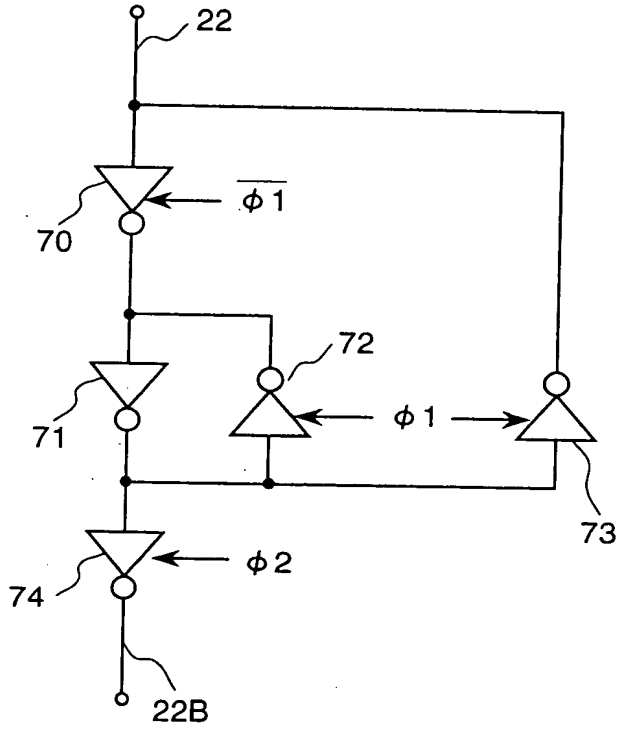

FIG. 15

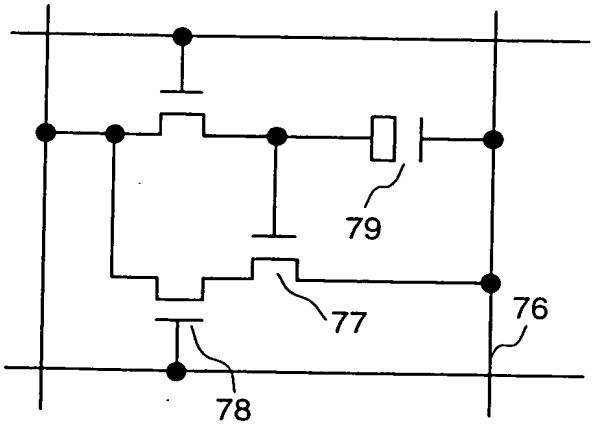

FIG. 11

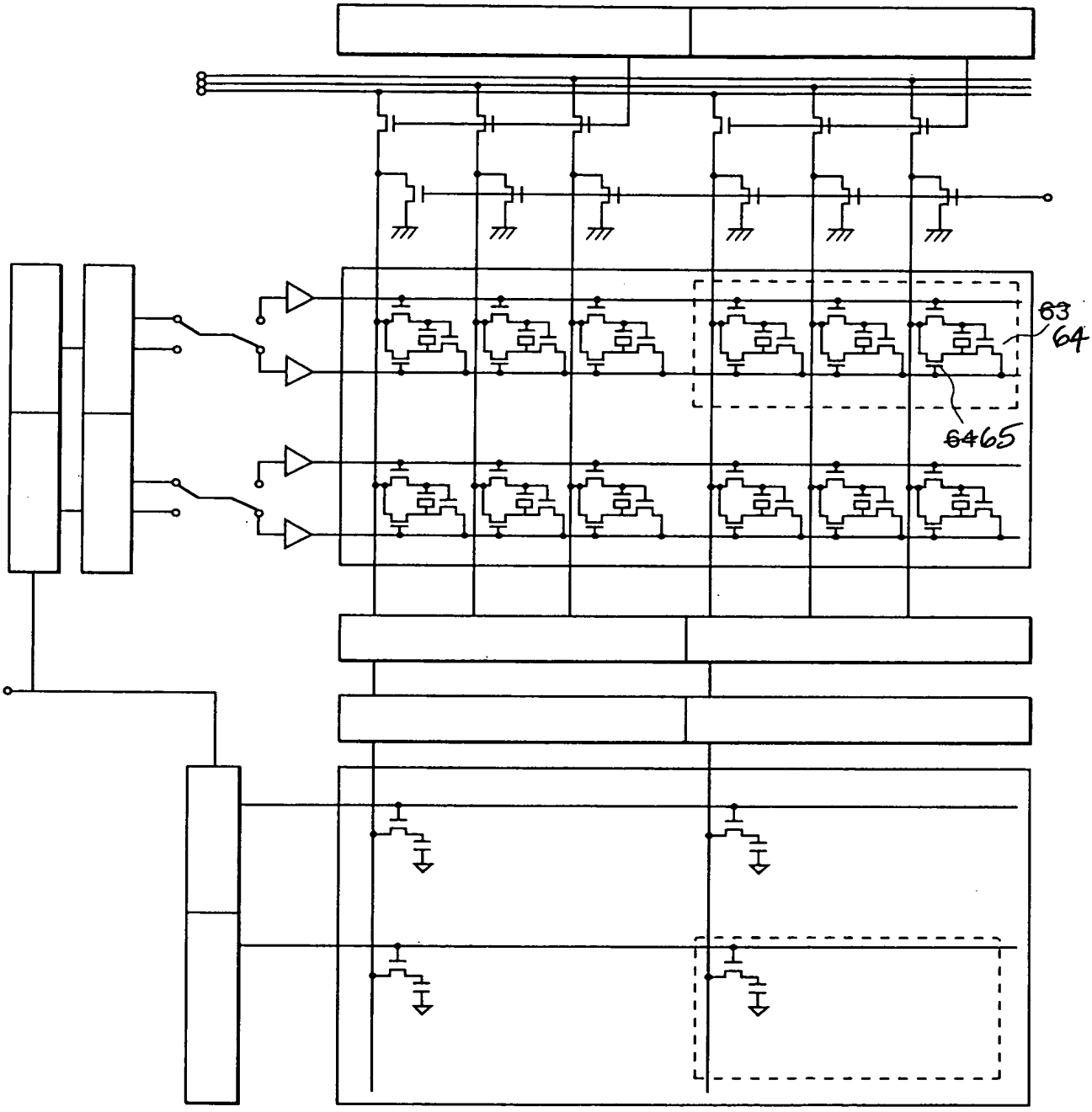

FIG. 12